What is claimed is:

[Claim 1] 1. A method for selectively scaling an integrated circuit design layout, the method comprising the steps of:

identifying a scaling target for at least one problem object of the design layout based on manufacturing information;

defining technology ground rules and methodology constraints for each problem object;

determining a scaling factor for each problem object;

determining which at least one of a plurality of scaling techniques is to be applied to each problem object, and scaling each problem object with a respective at least one scaling technique and scaling factor; and

in the case that assembly is required, performing placement and routing to assemble the design using the scaled problem object.

[Claim 2] 2. The method of claim 1, wherein the at least one problem object is selected from the group comprising: a layer, a region and a cell.

[Claim 3] 3. The method of claim 1, wherein the placement and routing performing step includes using an optimization-based hierarchical scaling program to produce a legal layout for each problem object.

[Claim 4] 4. The method of claim 1, wherein the scaling factor is at least one of: a compensation, a new ground rule and a scaling multiplier.

[Claim 5] 5. The method of claim 1, wherein the identifying step includes:

manufacturing the design layout;

testing the manufactured design layout and identifying at least one problem object that is a problem; and
generating the manufacturing information.

[Claim 6] 6. The method of claim 5, wherein the testing step includes characterizing operation and identifying the at least one problem object by obtaining data indicating how well objects are able to be manufactured.

[Claim 7] 7. The method of claim 5, wherein the manufacturing information generating step includes generating the scaling target for the problem object.

[Claim 8] 8. The method of claim 1, further comprising the step of evaluating whether a new design layout including the scaled objects achieves an expected behavior.

[Claim 9] 9. A system for selectively scaling an integrated circuit design layout, the system comprising the steps of:

means for identifying a scaling target for at least one problem object of the design layout based on manufacturing information;

means for defining technology ground rules and methodology constraints for each problem object;

means for determining a scaling factor for each problem object;

means for determining which at least one of a plurality of scaling techniques is to be applied to each problem object, and scaling each problem object with a respective at least one scaling technique and scaling factor; and

means for, in the case that assembly is required, performing placement and routing to assemble the design using the scaled problem object.

[Claim 10] 10. The system of claim 9, wherein the at least one problem object is selected from the group comprising: a layer, a region and a cell.

[Claim 11] 11. The system of claim 9, wherein the placement and routing performing means includes means for conducting an optimization-based hierarchical scaling to produce a legal layout for each problem object.

[Claim 12] 12. The system of claim 9, wherein the scaling factor is at least one of: a compensation, a new ground rule and a scaling multiplier.

[Claim 13] 13. The system of claim 9, wherein the identifying means includes:

means for testing a manufactured design layout and identifying at least one problem object that is a problem; and

means for generating the manufacturing information.

[Claim 14] 14. The system of claim 13, wherein the testing means includes means for characterizing operation and identifying the at least one problem object by obtaining data indicating how well objects are able to be manufactured.

[Claim 15] 15. The system of claim 13, wherein the manufacturing information generating means includes means for generating the scaling target for the problem object.

[Claim 16] 16. The system of claim 13, further comprising means for evaluating whether a new design layout including the scaled objects achieves an expected behavior.

[Claim 17] 17. A computer program product comprising a computer useable medium having computer readable program code embodied therein for selectively scaling an integrated circuit design layout, the program product comprising:

program code configured to identify a scaling target for at least one problem object of the design layout based on manufacturing information;

program code configured to define technology ground rules and methodology constraints for each problem object;

program code configured to determine a scaling factor for each problem object;

program code configured to determine which at least one of a plurality of scaling techniques is to be applied to each problem object, and scaling each problem object with a respective at least one scaling technique and scaling factor; and

program code configured to, in the case that assembly is required, perform placement and routing to assemble the design using the scaled problem object.

[Claim 18] 18. The program product of claim 17, wherein the at least one problem object is selected from the group comprising: a layer, a region and a cell.

[Claim 19] 19. The program product of claim 17, wherein the placement and routing performing code includes program code configured to conduct an optimization-based hierarchical scaling to produce a legal layout for each problem object.

[Claim 20] 20. The program product of claim 17, wherein the scaling factor is at least one of: a compensation, a new ground rule and a scaling multiplier.

[Claim 21] 21. The program product of claim 17, wherein the identifying code includes:

program code configured to test a manufactured design layout and identify at least one problem object that is a problem; and
program code configured to generate the manufacturing information.

[Claim 22] 22. The program product of claim 21, wherein the testing code includes program code configured to characterize operation and identify the at least one problem object by obtaining data indicating how well objects are able to be manufactured.

[Claim 23] 23. The program product of claim 17, wherein the manufacturing information generating code includes program code configured to generate a scaling target for the problem object.

[Claim 24] 24. The program product of claim 17, further comprising program code configured to evaluate whether a new design layout including the scaled objects achieves an expected behavior.

[Claim 25] 25. A method for improving yield of an integrated circuit design layout during manufacturing, the method comprising the steps of:

testing a manufactured design layout and identifying at least one problem object that is a problem;

generating manufacturing information obtained during the testing; and

feeding back the manufacturing information to a system for selective scaling of the design layout to improve yield using a scaling target for at least one problem object of the design layout based on the manufacturing information.

[Claim 26] 26. The method of claim 25, wherein the testing step includes characterizing operation by obtaining data indicating how well objects are able to be manufactured.

[Claim 27] 27. A system for improving yield of an integrated circuit design layout during manufacturing, the system comprising:

means for testing a manufactured design layout and identifying at least one problem object that is a problem;

means for generating manufacturing information including a scaling target for each problem object; and

means for feeding back the manufacturing information to a system for selective scaling of the design layout to improve yield using a scaling target for at least one problem object of the design layout based on the manufacturing information.

[Claim 28] 28. The system of claim 27, wherein the testing means includes means for characterizing operation by obtaining data indicating how well objects are able to be manufactured.

[Claim 29] 29. A computer program product comprising a computer useable medium having computer readable program code embodied therein for improving yield of an integrated circuit design layout during manufacturing, the program product comprising:

program code configured to test a manufactured design layout and identifying at least one problem object that is a problem;

program code configured to generate manufacturing information including a scaling target for each problem object; and

program code configured to feed back the manufacturing information to a system for selective scaling of the design layout to improve yield using a scaling target for at least one problem object of the design layout based on the manufacturing information.

[Claim 30] 30. The program product of claim 29, wherein the testing code includes program code configured to characterize operation by obtaining data indicating how well objects are able to be manufactured.